MULTIPLICATION LOGIC CIRCUIT

ABSTRACT

A multiplication logic circuit comprises array generation logic and array reduction logic. The array reduction logic comprises array reduction logic for a first level of array reduction which comprises maximal length parallel counters for reducing maximal length columns. The output of the maximal length parallel counters are then further reduced by a second level of reduction logic comprising logic circuits with asymmetric delays in order to compensate for the differential delays experienced by the outputs of the maximal length parallel counters.